CLAIMS

What is claimed is:

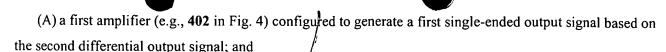
- 1. An interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:
- (a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the low-frequency impedance of the tip/ring lines;
 - (b) high-frequency interface circuitry configured to process the high-frequency signals; and
 - (c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:
 - (1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines;
 - (2) a coder/decoder (CODEC) configured to encode and decode the low-frequency signals; and
 - (3) an impedance warping circuit (IWC) configured between the SLIC and the CODEC, wherein the IWC tends to compensate for the effect of the blocking capacitor on the low-frequency impedance between the tip/ring lines.
 - 2. The invention of claim 1, wherein the compensation provided by the IWC provides a desired impedance between the tip/ring lines for both the low-frequency and high-frequency signals.
 - 3. The invention of claim 2, wherein the desired impedance has a resistance of about 900 ohms and a capacitance of about 2.16 microfarads.
 - 4. The invention of claim 1, wherein:
 the high-frequency signals correspond to DSL signals having frequencies greater than about 4 kHz;
 the low-frequency signals correspond to PDTS signals having frequencies less than about 4 kHz; and
 the filter circuitry comprises (i) a high-pass filter configured to provide the DSL signals to the highfrequency interface circuitry and (ii) a low-pass filter configured to provide the POTS signals to the lowfrequency interface circuitry, wherein the blocking capacitor is part of the high-pass filter.
- 5. The invention of claim 1, wherein the IWC is configured to receive a first differential signal (e.g., VRTX, VTX of Figs. 3-4) from the SLIC and a second differential signal from the CODEC (e.g., VRN, VRP of Figs. 3-4) and generate a third differential signal provided to the SLIC (e.g., RCVN, RCVP of Figs. 3-4).
 - 6. The invention of claim 5, wherein the IWC comprises:

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- (B) a second amplifier (e.g., **404** in Fig. 4) configured to generate a second single-ended output signal based on the first differential output signal, wherein the first and second single-ended output signals are used to generate the third differential output signal.
 - 7. The invention of claim 6, wherein:

the first amplifier comprises a first operational amplifier (e.g., 412) configured as an inverter; and the second amplifier comprises a second operational amplifier (e.g., 414) configured as a frequency-dependent inverter, such that the third differential output signal increases when frequency of the low-frequency signals increases.

- 8. The invention of claim 7, wherein the second amplifier further comprises a resistor (e.g., R7) and a compensating capacitor (e.g., C2) configured in parallel between the inverting input and the output of the second operational amplifier.
- 9. The invention of claim 6, wherein the IWC further comprises an output filter (e.g., **406** of Fig. 4) configured to filter the first single-ended output signal generated by the first amplifier.
- 10. An impedance warping circuit (IWC) for an interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:
- (a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the low-frequency impedance of the tip/ring lines;
 - (b) high-frequency interface circuitry configured to process the high-frequency signals; and
- (c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:
 - (1) a subscriber line interface circuit (\$LIC) configured between the tip and ring lines;
 - (2) a coder/decoder (CODEC) configured to encode and decode the low-frequency signals; and
- (3) the IWC configured between the SLIC and the CODEC, wherein the IWC tends to compensate for the effect of the blocking capacitor on the low-frequency impedance between the tip/ring lines.
- 11. The invention of claim 10, wherein the compensation provided by the IWC provides a desired impedance between the tip/ring lines for both the low-frequency and high-frequency signals.

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- 13. The invention of claim 10, wherein:
 the high-frequency signals correspond to DSL signals having frequencies greater than about 4 kHz;
 the low-frequency signals correspond to POTS signals having frequencies less than about 4 kHz; and
 the filter circuitry comprises (i) a high-pass filter configured to provide the DSL signals to the highfrequency interface circuitry and (ii) a low-pass filter configured to provide the POTS signals to the lowfrequency interface circuitry, wherein the blocking capacitor is part of the high-pass filter.
- 14. The invention of claim 10, wherein the IWC is configured to receive a first differential signal (e.g., VRTX, VTX of Figs. 3-4) from the SLIC and a second differential signal from the CODEC (e.g., VRN, VRP of Figs. 3-4) and generate a third differential signal provided to the SLIC (e.g., RCVN, RCVP of Figs. 3-4).
 - 15. The invention of claim 14, wherein the IWC comprises:
- (A) a first amplifier (e.g., **402** in Fig. 4) configured to generate a first single-ended output signal based on the second differential output signal; and
- (B) a second amplifier (e.g., 404 in Fig. 4) configured to generate a second single-ended output signal based on the first differential output signal, wherein the first and second single-ended output signals are used to generate the third differential output signal.
- 16. The invention of claim 15, wherein:
 the first amplifier comprises a first operational amplifier (e.g., 412) configured as an inverter; and
 the second amplifier comprises a second operational amplifier (e.g., 414) configured as a frequencydependent inverter, such that the third differential output signal increases when frequency of the lowfrequency signals increases.
- 17. The invention of claim 16, wherein the second amplifier further comprises a resistor (e.g., R7) and a compensating capacitor (e.g., C2) configured in parallel between the inverting input and the output of the second operational amplifier.
- 18. The invention of claim 15, wherein the IWC further comprises an output filter (e.g., 406 of Fig. 4) configured to filter the first single-ended output signal generated by the first amplifier.

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